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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,234	12/01/2003	Chin-Tien Yang	TSM03-0589	2127

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EXAMINER	
FORDE, REMMON R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

11-A

Office Action Summary	Application No.	Applicant(s)	
	10/725,234	YANG ET AL.	
	Examiner	Art Unit	
	Remmon R. Fordé	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *23-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response To Election

Applicant's election of Group I: Claims 1-22 in correspondence dated 01/05/05 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-8, 10-14 and 16-21 rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al..

Regarding claim 1, referencing Figures 5-7, Chang et al. discloses a twin bit cell flash memory device (100) that is provided with a substrate (82) defining at least one channel region (101) separating areas of buried diffusion (97 & 99); a bottom dielectric (84) formed over the channel region and having a first edge and a second edge; a data storage layer (86) formed over the bottom dielectric, the data storage layer comprising a middle dielectric (87) covering an intermediate portion of the bottom dielectric, a first

floating gate (70) extending over the bottom dielectric from the first edge to the middle dielectric and a second floating gate (70) extending over the bottom dielectric from the second edge to the middle dielectric; a top dielectric (90) covering the data storage layer; and a gate electrode (91/92) formed over the top dielectric. (Column 2, line 66 – column 4, line 30.)

Regarding claim 3, referencing Figures 5-7, Chang et al. further discloses that the bottom dielectric (84) is silicon oxide. (Column 3, lines 4-8.)

Regarding claim 4, referencing Figures 5-7, Chang et al. further discloses that the top dielectric (90) is silicon oxide. (Column 3, lines 34-36.)

Regarding claims 5 and 6, referencing Figures 5-7, Chang et al. further discloses that the middle dielectric (87) is silicon nitride. (Column 3, lines 24-27.)

Regarding claim 7, referencing Figures 5-7, Chang et al. further discloses that the bottom dielectric (84) has a thickness of between about 70 and about 100 angstroms (i.e. 50 to 150 angstroms). (Column 3, lines 4-8.)

Regarding claim 8, referencing Figures 5-7, Chang et al. further discloses that the top dielectric (90) has a thickness of between about 70 and about 100 angstroms (i.e. 50 to 150 angstroms). (Column 3, lines 34-36.)

Regarding claim 10, referencing Figures 5-7, Chang et al. further discloses that the gate electrode (91/92) is a layer of polysilicon. (Column 3, lines 48-61.)

Regarding claims 11-13, referencing Figures 5-7, Chang et al. further discloses that the first and second floating gates (70) are made of polysilicon. (Column 3, lines 8-12.)

Regarding claim 14, referencing Figures 5-7, Chang et al. further discloses an ONO semiconductor device (100) for storing dual data bits provided with a substrate (82) defining at least one channel region (101) separating areas of buried diffusion (97&99); a first oxide dielectric (84) formed over the channel region and having a first edge and a second edge; a data storage layer (86) formed over the first oxide dielectric layer (84), the data storage layer comprising a nitride dielectric layer (87) covering an intermediate portion of the first oxide dielectric layer, a first polysilicon floating gate (70) extending over the oxide dielectric layer from the first edge to the nitride dielectric and a second polysilicon floating gate (70) extending over the oxide dielectric layer from the second edge to the nitride dielectric; a second oxide dielectric layer (90) covering the data storage layer; and a polysilicon layer (91/92) formed over the second oxide dielectric layer. (Column 2, line 66 – Column 4, line 30.)

Regarding claim 16, referencing Figures 5-7, Chang et al. further discloses that the first oxide layer (84) is silicon oxide. (Column 3, lines 4-8.)

Regarding claim 17, referencing Figures 5-7, Chang et al. further discloses that the second oxide layer (90) is silicon oxide. (Column 3, lines 34-36.)

Regarding claims 18 and 19, referencing Figures 5-7, Chang et al. further discloses that the nitride layer (87) is silicon nitride. (Column 3, lines 24-27.)

Regarding claim 20, referencing Figures 5-7, Chang et al. further discloses that the first oxide layer (84) has a thickness of between about 70 and about 100 angstroms (i.e. 50 to 150 angstroms). (Column 3, lines 4-8.)

Regarding claim 21, referencing Figures 5-7, Chang et al. further discloses that the second oxide layer (90) has a thickness of between about 70 and about 100 angstroms (i.e. 50 to 150 angstroms). (Column 3, lines 34-36.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Ahmad et al..

Referencing Figures 5-7, Chang et al. discloses a twin bit cell flash memory device (100) that is provided with a substrate (82) defining at least one channel region (101) separating areas of buried diffusion (97 & 99); a bottom dielectric (84) formed over the channel region and having a first edge and a second edge; a data storage layer (86) formed over the bottom dielectric, the data storage layer comprising a middle dielectric (87) covering an intermediate portion of the bottom dielectric, a first floating gate (70) extending over the bottom dielectric from the first edge to the middle dielectric and a second floating gate (70) extending over the bottom dielectric from the second edge to the middle dielectric; a top dielectric (90) covering the data storage layer; and a gate electrode (91/92) formed over the top dielectric. (Column 2, line 66 – column 4, line 30.)

Chang et al. fails to disclose providing spacers to be formed at the edges of the ONO and gate electrode stack.

However, referencing Figures 1-3, Ahmad et al. discloses providing sidewall spacers on the sides of a FET structure. Ahmad et al. further teaches that the sidewall spacers protect the gate structures during subsequent processing steps and that the use of sidewall spacers is conventional. (Column 1, lines 30-52.)

Since Ahmad et al. and Chang et al. are from the same field of endeavor, the purpose as disclosed by Ahmad et al would have been recognized in the pertinent of Chang et al..

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to improve the memory device as disclosed by Chang et al. and use sidewall spaces because Amad et al. teaches that the sidewall spacers protect gate structures during subsequent processing steps and that the use of sidewall spacers is conventional. (Column 1, lines 30-52.)

Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Huseh.

Referencing Figures 5-7, Chang et al. discloses a twin bit cell flash memory device (100) that is provided with a substrate (82) defining at least one channel region (101) separating areas of buried diffusion (97 & 99); a bottom dielectric (84) formed over the channel region and having a first edge and a second edge; a data storage layer (86)

formed over the bottom dielectric, the data storage layer comprising a middle dielectric (87) covering an intermediate portion of the bottom dielectric, a first floating gate (70) extending over the bottom dielectric from the first edge to the middle dielectric and a second floating gate (70) extending over the bottom dielectric from the second edge to the middle dielectric; a top dielectric (90) covering the data storage layer; and a gate electrode (91/92) formed over the top dielectric. (Column 2, line 66 – column 4, line 30.)

Chang et al. fails to disclose providing that the middle dielectric layer has a thickness of between about 50 and 70 angstroms.

However, referencing Figures 3A – 4, Huseh discloses a ONO structure for use in a memory device, wherein the middle dielectric layer (104) has a thickness of 50-60 angstroms and the sandwiching oxide layers (102) and (106) being made with a thickness of 50-70 angstroms and 80-100 angstroms respectively. (Column 2, lines 45-50.)

It would have been obvious at the time the invention was made to one of ordinary skill in the art to improve the memory device as disclosed by Chang et al. by providing a middle dielectric layer with a thickness of between about 50-60 angstroms as disclosed by Huseh for the purpose of providing the middle dielectric layer with reduced dimensions to aid in the miniaturization of the memory device.

Relevant Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Eitan, Lin et al., Bloom et al. and Huang et al. each disclose semiconductor memory devices.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Remmon R. Fordé whose telephone number is (571) 272-1916. The examiner can normally be reached on Monday-Thursday (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Remmon R. Fordé